Effect of Impact Ionization and Carrier Multiplication on Graphene MOSFET at different dimensions

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***Abstract*— This work reports that the effect of carrier multiplication as well as carrier generation by impact ionization is non-negligible due to the absence of band gap on Graphene. Here, an extended version of charge control model is proposed in which the carrier generation rate is considered and solved self-consistently with drain source voltage. However, the effects of using different dielectrics as top gate oxide along with device dimensions on the I-V characteristics of graphene MOSFET are compared. Better drain saturation current of 12 mA is obtained at proper choice of dielectric (HfO_2) and device dimensions in comparison with reference work [7]. In addition, a significant down-kick on the I-V characteristics beyond pinch off is observed which signatures the effect of carrier multiplication in Graphene.**

***Keywords*— graphene MOSFET, large area graphene, carrier multiplication, extended charge control model, device dimensions.**

I. Introduction

Graphene a flat mono layer of sp^2 carbon atoms tightly packed into a two dimensional (2D) honeycomb lattice is a rising star on the horizon of material science due to its exceptional electronic properties such as high carrier mobility, current densities larger than 10^8A/cm^2, low resistivity and high thermal conductivity at room temperature [1]-[5]. Due to its high carrier mobility and ultrathin body, graphene has attracted tremendous attention as a channel material for future high speed nano-electronic device. Graphene based devices are now considered as an option for a post Si electronics [6].

The progress in the development of graphene transistors is breathtaking. Since large-area graphene has no band gap. Moderate electric fields can cause carrier generation by impact ionization. Impact ionization is essentially the reverse of the Auger recombination process which originates from the Coulomb interaction between carriers [4], [7]. In this process, a highly energetic conduction band electron colliding with a valence band electron gives two conduction electrons and a hole [7]. This work reports that carrier generation by impact ionization has a non-negligible effect due to the vanishing energy gap in graphene.

In earlier carrier multiplication effect on I-V characteristics was observed at fixed W = 2μm, L = 1μm, μ_o=2000cm^{2}V^{-1}s^{-1}, t_{ox} = 20nm, V_T = 0.5V & oxide was SiO_2 [7] which is not sufficient for understanding the device performance clearly, i.e. the drain current(2mA) and generation rate are low due to low dielectric constant of gate oxide. The use of high dielectric oxide plays a vital role to enhance the generation rate as well as device performance of graphene MOSFET. In this paper, it is shown that high gate dielectric oxide and high electric field results better I-V characteristics in graphene MOSFET in comparison with [7].

II. Device structure

A Graphene metal-oxide field-effect transistor (G- MOSFET) is shown in Fig.1, where the channel layer is made of single layer graphene. The working principle is the same of MOSFET device but, due to the ambipolar nature of graphene, according to the sign of the gate voltage, we will have the device working with electrons (n transistor, $V_{GT} > 0$) or holes (p transistor, $V_{GT} < 0$) [7]. The length and width of the graphene channel are assumed as 5 μm and 2 μm respectively. Here, HfO_2 (k=9) is used as top gate oxide.

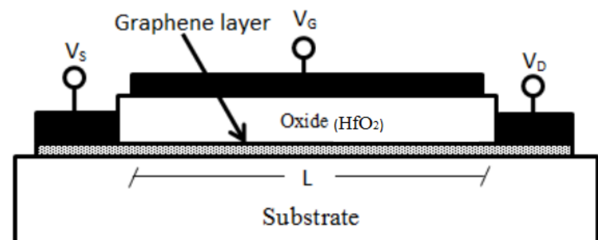

Figure 1: Graphene as a channel in MOSFET [7]

III. CHARGE CONTROL MODEL

Considering an n- MOSFET operating in above threshold regime, with a gate voltage that is sufficiently high to cause the inversion in the entire length of the channel at zero drain-source bias, we can describe the mobile inversion charge in a quite general way as [5]

$$Q_{+} + Q_{-} = -C_{0x}(V_{GT} - v(x)) \tag{1}$$

where Q_{+} and Q_{-} are the hole and electron charges in the channel respectively, C_{ox} is the oxide capacitance, $V_{GT} = V_G - V_T$ and V(x) is the potential drop in side the channel . The sign is for electron (+) and hole (-) channels. Finally we get the device current as [8],

$$C_{0x}\mu_0 w(V_{GT} - v(x))F = I \tag{2}$$

It is possible to integrate eq. (2) along all the channel length [7], [8], and get the expression for the total current in the transistor.

$$I = \frac{C_{0x}\mu_0 w[V_{GT}V_{DS} - V_{DS}{}^2]}{L} \tag{3}$$

One can obtain the equation of electric potential from eq. (3) [7] as,

$$v(x) = V_{GT} - \sqrt{V_{GT}{}^2 - \frac{2Ix}{C_{0x}\mu_0 w}} \tag{4}$$

The derivation of eq. (4) respect to *x* position yields to find the electric field in the channel [5]

$$F(x) = -\frac{I}{C_{0x}\mu_0 w\sqrt{V_{GT}{}^2 - \frac{2Ix}{C_{0x}\mu_0 w}}} \tag{5}$$

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IV. INCLUDE GENERATION RATE IN CHARGE CONTROL MODEL

The continuity equations with the generation rate eq. become [7]

$$\frac{dI_n{}^{drift}}{dx} + ew\frac{U}{2} = 0 \tag{6}$$

$$\frac{dI_p{}^{drift}}{dx} + ew\frac{U}{2} = 0 \tag{7}$$

here, generation rate equation can be written as ,

$$U = gF^{\alpha}\exp[-(\frac{n}{n_0})] \tag{8}$$

where the factor 2 accounts the generation both of electrons and holes. For simplicity, we can define the generation of electrons that is equal in magnitude to the generation for holes $G(x) = \frac{U(x)}{2}$. Solving eq. (6) and (7) we will get

$$I = I_p{}^{drift} - I_n{}^{drift} - 2ew\int_x^L G(x)dx \tag{9}$$

where I is the positive electron current. In this case, we define the carrier velocity, taken equal for electrons and holes due to the symmetry in the band structure in graphene as [7]

$$v(F(x)) = \pm\frac{\mu_0 F(x)}{1 + \frac{F(x)}{F_c}} \tag{10}$$

where F_C is the saturated field along channel and the low field mobility μ_o has used and get the expression for the total current in the transistor depending of V_{DS},

$$I = \frac{C_{0x}\mu_0 w[V_{GT}V_{DS} - V_{DS}{}^2]}{L(1 + \frac{V_{DS}}{V_c})} + \frac{2ew}{1 + \frac{V_{DS}}{V_c}}\int_0^L (1 - \frac{x'}{L} + \frac{V_{DS} - v(x)}{V_c})G(x')dx \tag{11}$$

where $V_C = F_C L$. Finally, we get the expression of the current inside the channel including also the generation rate additionally, eq. (10) & we get the potential inside the channel.

$$v(x) = \{V_{GT} - V_i + \frac{2e}{F_c C_{0x}\mu_0}\int_0^L G(x')dx' - \sqrt{[V_{GT} - V_i + \frac{2e}{F_c C_{0x}\mu_0}\int_0^L G(x')dx']^2 - 2F_c V_i x + \frac{4e}{C_{0x}\mu_0}\int_0^x [x - x' + \frac{v(x)}{F_c}]G(x')dx'}\} \tag{12}$$

where $V_i = \frac{I}{F_c C_{0x}\mu_0 w}$. Deriving eq. (12) with respect to the position we get the electric field [4], [5].

$$F(x) = -\{\frac{2eG(x)}{F_c C_{0x}\mu_0} - \frac{\frac{2eG(x)}{F_c C_{0x}\mu_0}[V_{GT} - V_i - v(x) + \frac{2e}{F_c C_{0x}\mu_0}\int_0^x G(x')dx'] + \frac{2e}{C_{0x}\mu_0}\int_0^x G(x')dx - F_c V_i}{\sqrt{[V_{GT} - V_i + \frac{2e}{F_c C_{0x}\mu_0}\int_0^L G(x')dx']^2 - 2F_c V_i x + \frac{4e}{C_{0x}\mu_0}\int_0^x [x - x' + \frac{v(x)}{F_c}]G(x')dx'}}\} \tag{13}$$

V. RESULTS AND DISCUSSION

In order to illustrate the effects of carrier multiplication in graphene, we have consider a Graphene MOSFET with the following standard parameters: W = 5μm, L = 2μm, μ_o=2000cm^{2}V^{-1}s^{-1}, t_{ox} = 20nm, V_T = 0.5V & oxide is HfO_2 for high saturation drain current. Even if we performed simulation in case of n channel (positive top gate voltage) and positive drain source bias, the model is valid also for holes as well.

Fig. 2(a) shows the net generation rate along the channel for different drain biases at a fixed gate voltage V_{GT} = 3V, which

increases with the drain source voltage as expected. It is clear that a high generation rate is observed towards the drain end at high drain source voltage.

Fig. 2(b) shows the variation of hole concentration as a function of the source - drain voltage for three top gate biases. The minimum value of carrier concentration has been shifted towards right with increasing gate voltage.

Fig. 2(c) shows the comparison between our work and the previous work [7]. The blue (HfO_2) and red (Al_2O_3) colour represent our work where green colour (SiO_2) represents the reference work [7] respectively. The value of drain saturation current is obtained approximately as 8.5mA and 5mA respectively which are higher than 2 mA [7] respectively. This is due to the effect of carrier multiplication. So, the use of HfO_2 as a dielectric oxide is promising. It is also shown that a significant down-kick current is obtained at high drain bias beyond pinch off.

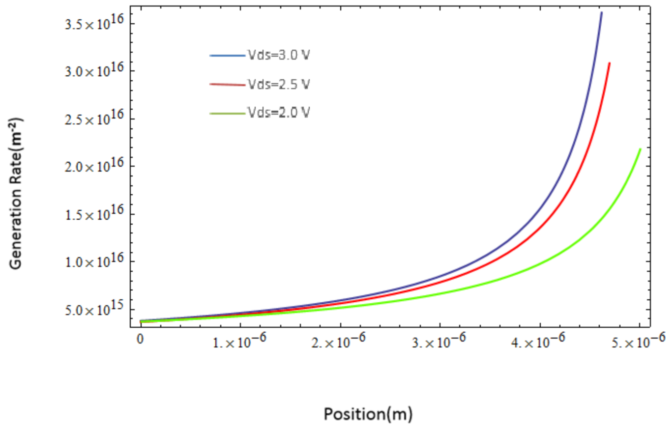

Fig. 2(a) Net generation rate as a function of position for different values of V_{DS} =2.0V, 2.5V and 3.0V.

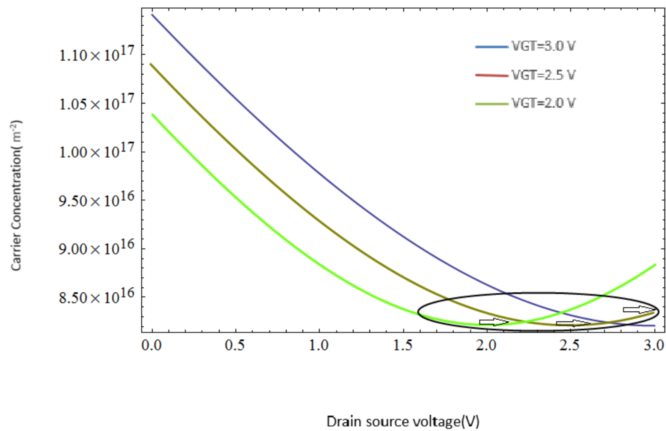

Fig. 2(b) Carrier concentration as a function of source drain voltage.

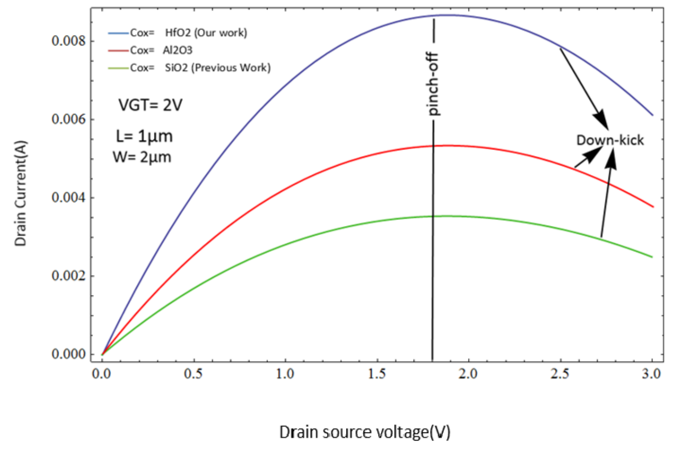

Fig. 2(c) Drain current as a function of drain source voltage for different oxides HfO_2, Al_2O_3 & SiO_2 at V_{GT} =2.0V.

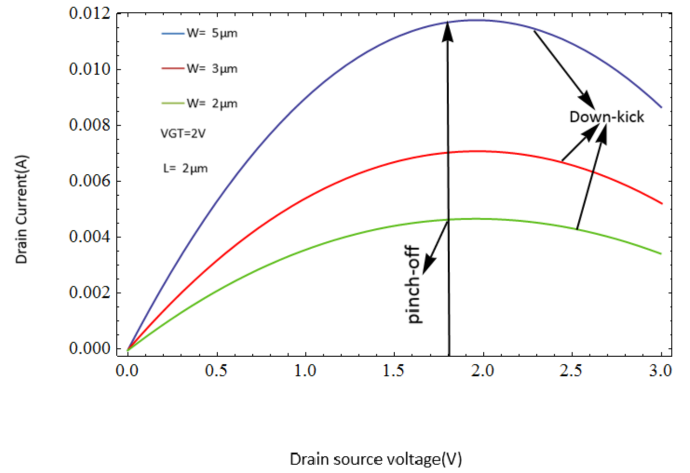

Fig. 2(d) Drain current as a function of drain source voltage for different device widths at V_{GT} =2.0V.

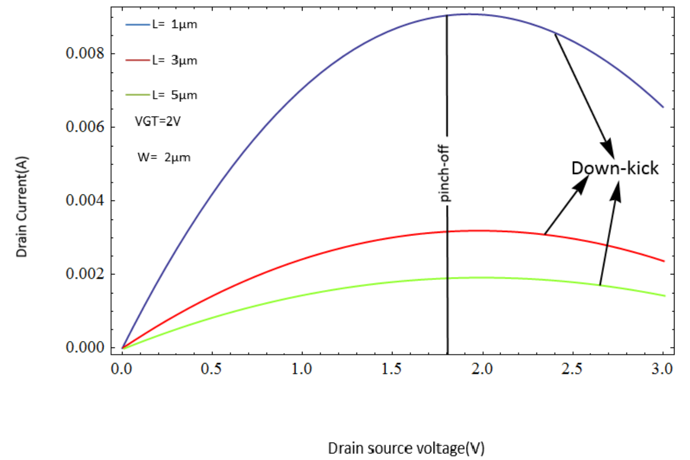

Fig. 2 (e) Drain current as a function of drain source voltage for different device lengths at V_{GT} =2.0V.

Fig. 2(d) shows that the effect of carrier multiplication on the I-V characteristics of the transistor for three values of width at fixed value of gate voltage, V_{GT}=2V and fixed length 2µm. Here it is clear that if width of graphene is increased, the saturation current at beyond pinch-off will be increased. High saturation current of 12mA is observed with increasing width of 5µm better than the published results in [7] that found to be 2mA. In addition, a significant down-kick in the drain current characteristics is also observed beyond pinch-off.

Fig. 2(e) displays that the effect of carrier multiplication on the I-V characteristics of the transistor for three values of graphene length from 1µm-5µm at constant value of gate voltage, V_{GT}=2V and fixed width 2µm. Here it is clear that if device length of graphene is increased, the saturation current at beyond pinch-off is decreased.

VI. CONCLUSIONS

In this paper, the effects of using different dielectrics as top gate oxide along with device dimensions on the I-V characteristics of graphene MOSFET has been simulated and compared. The optimum value of drain saturation current depends on proper choice of dielectric as well as device dimensions. At graphene width, W = 5µm and length, L = 2µm with HfO_2 (k=9) as dielectric, the maximum value of drain saturation current is found as 12mA which is promising and better than results obtained in [7].

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