# Analysis of Device Performance of a Heterojunction Solar Cell with Amorphous Intrinsic Thin Layer (HIT) based on Device Parameters

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***Abstract*— A simulation based analysis of device performance of a HIT solar cell owing to varied device parameters has been presented in this work. Major electrical properties of a solar cell like open circuit voltage, short circuit current density, maximum power output from the cell, conversion efficiency and fill factor have been determined for variation in major device parameters like thickness of intrinsic and doped amorphous silicon layers, doping concentration of crystalline bulk, n and p-doped layers, work function of contact TCO etc. and simulated results have been analyzed altogether to find the optimized device parameters. All the simulation work has been accomplished using commercially available 2D device simulator ATLAS.**

***Keywords*— Amorphous intrinsic layer, TCO, open circuit voltage, short circuit current, conversion efficiency**

## I. INTRODUCTION

Heterojunction solar cell with amorphous intrinsic thin layer (HIT) is a promising heterojunction device structure in terms of low manufacturing cost and high conversion efficiency [1]-[7]. The device also bids fair to be a potential candidate for solar energy industry for its high stability characteristic [8]. Wide band gap of amorphous silicon (1.55-1.87eV) increases the external quantum efficiency of the solar cell device especially at lower wavelengths where most concentrated intensity of the terrestrial solar radiation can be found [9]. Inclusion of two intrinsic amorphous silicon layers which sandwich the crystalline bulk, ensure significant improvement in terms of open circuit voltage and conversion efficiency [10].

In our work, a simulation study of the device performance of HIT solar cell based on basic device parameters has been presented. We have focused on optimizing device parameters like thickness, doping concentrations; contact work function etc. of various layers of the heterojunction device by analyzing simulation results of major electrical properties like open circuit voltage, short circuit current density, maximum power output from the cell, conversion efficiency and fill factor of the device. 2D device simulator ATLAS was used for simulating all the electrical properties of the device.

## II. DEVICE STRUCTURE

The device structure of the HIT solar cell has been presented in Fig. 1. The light receiving front surface is of Transparent Conductive Oxide (TCO). Rear surface is also formed of the same material. The thickness of the front and the rear TCO surface are 70nm and 200nm respectively. The layer next to front TCO is of p-doped hydrogenated amorphous silicon [a:Si:H (p)] (10nm) which is followed by an intrinsic layer of hydrogenated amorphous silicon [i-Si:H ] (7nm) and a n-doped crystalline silicon [c-Si] bulk (100μm). An intrinsic layer of hydrogenated amorphous silicon (20nm) is inserted underneath the c-si bulk, next to which is a layer of n-doped hydrogenated amorphous silicon [a:Si:H (n)] (35nm) just above the rear TCO surface. Doping concentrations of a:Si:H (p), c-Si and a:Si:H (n) are $2x10^{19}/cm^3$, $1x10^{17}/cm^3$ and $2x10^{19}/cm^3$ respectively.

## III. SIMULATION PARAMETERS AND SIMULATION MODELS

For simulating electrical properties of HIT Solar cell in 2D device simulator ATLAS, a fine, two dimensional grid called mesh [11] was defined with a finer grid lines at the device interfaces. In the defined mesh structure, material regions have been defined with the corresponding doping

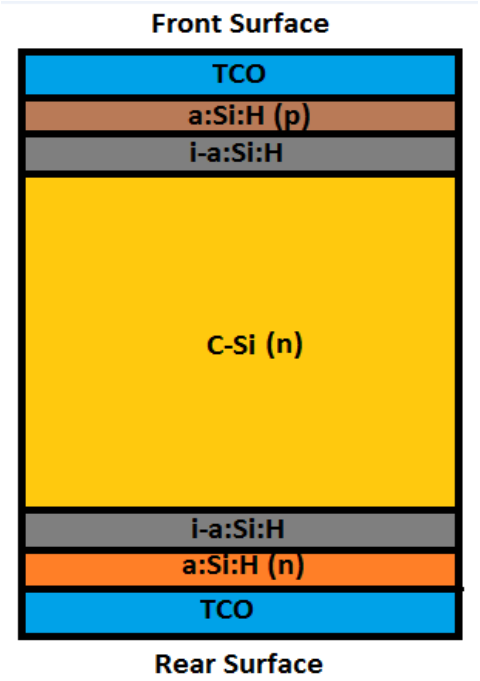


Fig. 1. Device structure of the HIT Solar Cell

concentrations. Since disordered materials contain a large number of defect states within the band gap of the material, for accurate modeling of the HIT solar cell device containing polycrystalline and amorphous materials, density of defects states has been defined as a combination of exponentially decaying band tail states and Gaussian distributions of mid-gap states. The total density of states, $g(E)$ can be expressed as :

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (1)$$

where, $g_{TA}(E)$, $g_{TD}(E)$, $g_{GA}(E)$ and $g_{GD}(E)$ are density of states for acceptor like conductor tail band, donor like valence tail band, deep level acceptor like band and deep level donor like band respectively. The last two are usually modeled using Gaussian distributions. The individual density of state can be expressed as:

$$g_{TA}(E) = (NTA)e^{\left(\frac{E-E_C}{WTA}\right)} \quad (2)$$

$$g_{TD}(E) = (NTD)e^{\left(\frac{E_V-E}{WTD}\right)} \quad (3)$$

$$g_{GA}(E) = (NGA)e^{\left[-\left(\frac{E_{GA}-E}{WGA}\right)^2\right]} \quad (4)$$

$$g_{GD}(E) = (NGD)e^{\left[-\left(\frac{E-E_{GD}}{WGD}\right)^2\right]} \quad (5)$$

where, $NTA$, $NTD$, $WTA$, $WTD$, $E_C$, $E_V$, $NGA$, $NGD$, $WGA$, $WGD$, $EGA$ and $EGD$ denote the conduction and valence band edge intercept densities, characteristic decay energy of conduction and valence band for an exponential tail distribution, conduction and valence band energy, deep level acceptor and donor like band edge intercept densities, characteristic decay energy and peak energy of acceptor and donor like band for Gaussian distribution.

Trapped carrier density has also been considered for accurate modeling of amorphous silicon layer. For steady state case, probability of occupation of a trap level at energy E for the tail and Gaussian acceptor and donor like states can be expressed as:

$$f_{TA} = \frac{v_n(SIGTAE)n + v_p(SIGTAH)n_i e^{\left(\frac{E_i-E}{kT}\right)}}{v_n(SIGTAE)\left[n + n_i e^{\left(\frac{E-E_i}{kT}\right)}\right] + v_p(SIGTAH)\left[p + n_i e^{\left(\frac{E_i-E}{kT}\right)}\right]} \quad (6)$$

$$f_{GA} = \frac{v_n(SIGGAE)n + v_p(SIGGAH)n_i e^{\left(\frac{E_i-E}{kT}\right)}}{v_n(SIGGAE)\left[n + n_i e^{\left(\frac{E-E_i}{kT}\right)}\right] + v_p(SIGGAH)\left[p + n_i e^{\left(\frac{E_i-E}{kT}\right)}\right]} \quad (7)$$

$$f_{TD} = \frac{v_p(SIGTDH)p + v_n(SIGTDE)n_i e^{\left(\frac{E-E_i}{kT}\right)}}{v_n(SIGTDE)\left[n + n_i e^{\left(\frac{E-E_i}{kT}\right)}\right] + v_p(SIGTDH)\left[p + n_i e^{\left(\frac{E_i-E}{kT}\right)}\right]} \quad (8)$$

$$f_{GD} = \frac{v_p(SIGGDH)p + v_n(SIGGDE)n_i e^{\left(\frac{E-E_i}{kT}\right)}}{v_n(SIGGDE)\left[n + n_i e^{\left(\frac{E-E_i}{kT}\right)}\right] + v_p(SIGGDH)\left[p + n_i e^{\left(\frac{E_i-E}{kT}\right)}\right]} \quad (9)$$

where, $v_n$, $v_p$, $n_i$, $SIGTAE$, $SIGGAE$, $SIGTAH$, $SIGGAH$, $SIGTDE$, $SIGGDE$, $SIGTDH$, $SIGGDH$ denote electron and hole thermal velocity, intrinsic carrier concentration, electron capture cross-section for the acceptor tail and Gaussian states, hole capture cross section for the acceptor tail and Gaussian states, electron capture cross-section for the donor tail and Gaussian states and hole capture cross section for the donor tail and Gaussian states respectively.

TABLE I
PARAMETERS USED FOR MODELING OF HYDROGENATED AMORPHOUS SILICON

| Parameter | i-a:Si:H | a:Si:H (n) | a:Si:H (p) |
|---|---|---|---|
| NTA($cm^{-3}$) | $1x10^{18}$ | $1x10^{21}$ | $1x10^{21}$ |
| NTD($cm^{-3}$) | $1x10^{18}$ | $1x10^{21}$ | $1x10^{21}$ |
| WTA(eV) | 0.06 | 0.07 | 0.07 |
| WTD(eV) | 0.09 | 0.12 | 0.12 |
| NGA($cm^{-3}$) | $1x10^{16}$ | $1x10^{19}$ | $1x10^{19}$ |
| NGD($cm^{-3}$) | $1x10^{16}$ | $1x10^{19}$ | $1x10^{19}$ |
| EGA(eV) | 1.1 | 0.7 | 1.3 |
| EGD(eV) | 0.9 | 0.45 | 1.1 |
| WGA(eV) | 0.15 | 0.2 | 0.2 |
| WGD(eV) | 0.15 | 0.2 | 0.2 |
| SIGGAE($cm^2$) | $1x10^{-16}$ | $1x10^{-16}$ | $1x10^{-16}$ |
| SIGGAH($cm^2$) | $1x10^{-14}$ | $1x10^{-14}$ | $1x10^{-14}$ |
| SIGGDE($cm^2$) | $1x10^{-14}$ | $1x10^{-14}$ | $1x10^{-14}$ |
| SIGGDH($cm^2$) | $1x10^{-16}$ | $1x10^{-16}$ | $1x10^{-16}$ |
| SIGTAE($cm^2$) | $1x10^{-17}$ | $1x10^{-17}$ | $1x10^{-17}$ |
| SIGTAH($cm^2$) | $1x10^{-15}$ | $1x10^{-15}$ | $1x10^{-15}$ |
| SIGTDE($cm^2$) | $1x10^{-15}$ | $1x10^{-15}$ | $1x10^{-15}$ |
| SIGTDH($cm^2$) | $1x10^{-17}$ | $1x10^{-17}$ | $1x10^{-17}$ |

Parameters used in our simulation for modeling hydrogenated amorphous silicon layer (both intrinsic and doped) have been listed in Table I.

The wide bandgap(1.75eV) of amorphous silicon has also been considered in our simulation. Carrier mobility and surface recombination velocity for electron and holes have been taken as 5 $cm^2V^{-1}s^{-1}$, 1 $cm^2V^{-1}s^{-1}$, 80$cms^{-1}$ and 80$cms^{-1}$ respectively. In the crystalline bulk, the resistivity is considered to be 1 Ωcm and minority carrier lifetime is set as 1ms[3]. Interface surface concentration of interface charge has been considered to be $1x10^{10}$ $cm^{-2}$.

For accurate modeling of the heterojunction device, we have used concentration and parallel field dependent mobility model, auger recombination model, band gap narrowing model, fowler-Nordheim tunneling and Thermoionic emission model in 2D Device simulator ATLAS.

## IV. Results and Analysis

In our simulation study, device performance of the HIT solar cell has been evaluated in terms of five basic electrical properties of a solar cell: Open Circuit Voltage, Short Circuit Current, Maximum power output, Conversion Efficiency and Fill factor for nine varying device parameters and the optimized parameters have been attained. In the following subsections, all the simulated results have been analyzed.

### *A. Effect of Intrinsic Amorphous Silicon Layer*

Conventional heterojunction solar cell [12] does not include intrinsic amorphous silicon layers on both the upper and lower part of the crystalline bulk. Inclusion of such two layers has significant effects on the device performance of the HIT solar cell which have been presented in Table II. It is obvious that inclusion of intrinsic layer increases open circuit voltage up to 734mV while it is 725mV without these layers. Short circuit current density also increases.There is also a rise in maximum power output from the cell and conversion efficiency thereby Fill factor is also enhanced to 78.75% from 75.78% due to the inclusion of two intrinsic amorphous silicon layers along with the conventional heterojunction device.

### *B. Effect of Crystalline Bulk Doping Concentration*

Fig. 3 shows the effect on open circuit voltage, short circuit current, maximum output power, conversion efficiency and fill factor of the HIT solar cell device for five different crystalline bulk doping concentrations. From Fig. 2(a), open circuit voltage increases with increasing doping concentrations, reach the peak (734mV) for $1x10^{17}cm^{-3}$ and concentrations. Short circuit current density, however, increases monotonically with the rise in doping concentrations and highest value of it is 32.13 $mA/cm^2$ for doping concentration of $1x10^{18}$ $cm^{-3}$ [Fig. 2(b)]. Maximum power output from the cell and highest conversion efficiency (20.58%) are attained at$1x10^{17}cm^{-3}$ [Fig. 2(c)-(d)]. In case of

TABLE II
Effect of Intrinsic Amorphous Silicon Layer on Device Performance

| Parameter | Solar Cell without intrinsic amorphous Si layer | Solar Cell with intrinsic amorphous Si layer |
|---|---|---|
| Open Circuit Voltage | 724mV | 734mV |
| Short Circuit Current Density | 29.55 $mA/cm^2$ | 30$mA/cm^2$ |
| Efficiency | 19.24% | 20.58% |
| Fill Factor | 75.78% | 78.75% |

Fill factor of device, identical characteristics to open circuit voltage are observed. Fill factor reaches maxima (78.75%) at doping concentration of $1x10^{17}cm^{-3}$ and become downwards again with lowest value of 70.28% at $1x10^{18}$ $cm^{-3}$ [Fig. 2(e)].

### *C. Effect of Front Intrinsic a:Si Layer Thickness*

Effect of front intrinsic amorphous Si layer thickness on various device parameters has been presented in Fig. 3 for five different layer thicknesses. Fig. 3(a) illustrates that with the increase of front a:Si layer thickness, open circuit voltage increases, while reverse characteristics are shown in case of short circuit current. With the increase in layer thickness, there is a decline in short circuit current density [Fig. 3(b)]. Maximum power output from the cell shows an increasing tendency from layer thickness 3 to 7 nm, reaches maxima at 7nm and from thereon, there is a linear fall in maximum output up to 11nm layer thickness [Fig. 3(c)]. Conversion efficiency curve shows an identical trend to max power output and highest efficiency attained with 7nm layer thickness is 20.59% [Fig. 3(d)]. There is a steady rise in Fill factor of the device up to 7nm layer thickness, but remains almost constant thereafter with the increase of a:Si layer thickness [Fig. 3(e)].

### *D. Effect of Rear intrinsic a:Si layer thickness*

Impact of varying rear intrinsic amorphous Si layer thickness on HIT solar cell performance has been presented in Fig. 4. Effect of variation in layer thickness is not much prominent in case of open circuit voltage. As seen from Fig. 4(a), open circuit voltage changes from 734.1mV to 734.5mV for layer thickness of 10nm to 20nm. Then there is again a slight decline in open circuit voltage which finally decreases to 734.1mV at 30nm layer thickness. Short circuit current density, however, decreases monotonically with increasing layer thickness and lowest value is found at 30nm thickness [Fig. 4(b)]. Maximum power output from the cell shows an increasing trend initially, reaches peak at 20nm layer thickness, then again falls with increasing layer thickness [Fig. 4(c)]. Similar curve characteristic is observed for conversion efficiency with highest conversion efficiency (20.59%) found at 20nm rear a:Si thickness[Fig. 4(d)]. Fill factor increases linearly with increasing thickness, becomes stable in the range 20-25nm and again increases up to 79.55% for 30nm layer thickness[Fig. 4(e)].

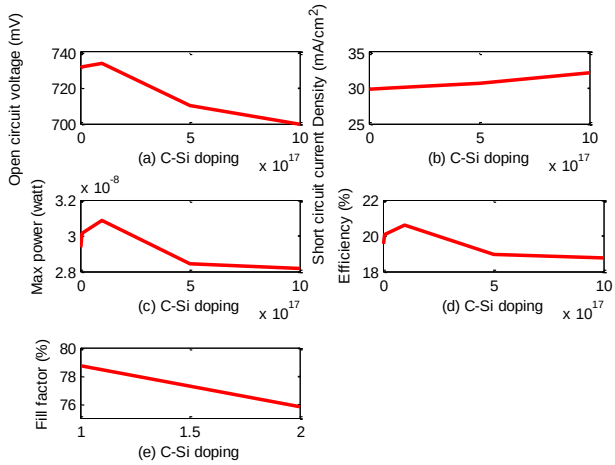


Fig. 2. Effect of crystalline silicon doping concentration on device performance

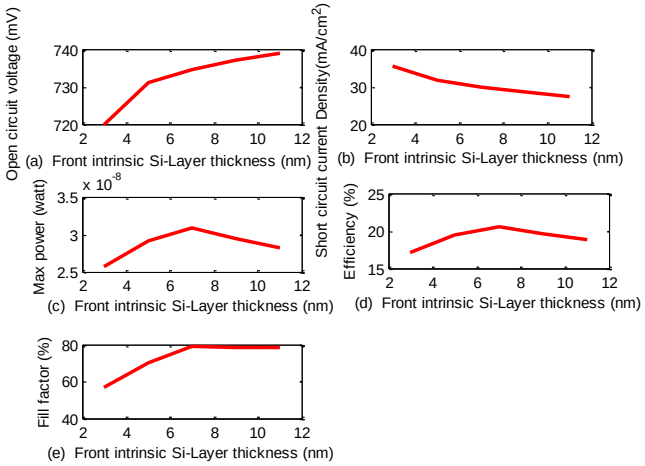


Fig. 3. Effect of front intrinsic a:Si layer thickness on device performance

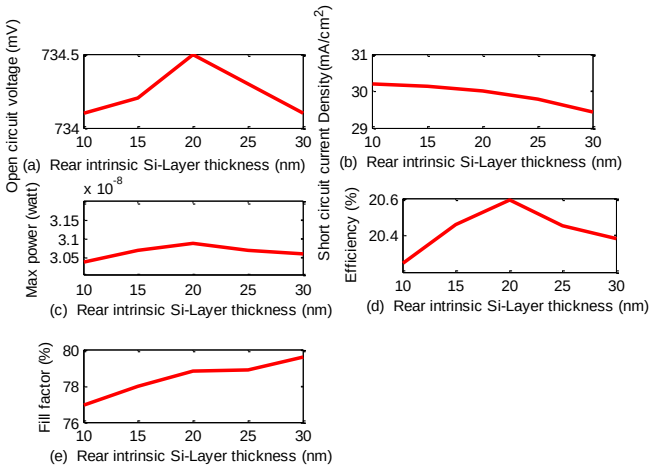


Fig. 4. Effect of rear intrinsic a:Si layer thickness on device performance

## *E. Effect of a:Si:H (p) layer doping concentration*

Effect of doping concentration of p-doped amorphous silicon layer on solar cell performance has been presented in Fig. 5 for seven different doping concentrations. Both open circuit voltage and short circuit current curves shows downward trends with increasing p-layer doping concentrations [Fig. 5(a)-(b)]. Open circuit voltage decreases significantly from 734.5mV to 713mV in the doping concentration range $2x10^{19}$ to $5x10^{19}$ $cm^{-3}$. Short circuit current density, however, has less steep downward characteristic with maxima at $2x10^{19}$ $cm^{-3}$ and minima at $5x10^{19}$ $cm^{-3}$. There is a gradual decline in maximum power output from the cell and conversion efficiency with increasing doping concentration [Fig. 5(c)-(d)] and maximum conversion efficiency (20.59%) is attained with p-type doping concentration of $2x10^{19}$ $cm^{-3}$. Fill factor, however, improves as the p-layer doping concentration is increased and reaches the peak (80.16%) for doping concentration of $5x10^{19}$ $cm^{-3}$ [Fig. 5(e)].

## *F. Effect of a:Si:H (p) layer thickness*

Impact of varying p-doped amorphous Si layer thickness on device performance has been presented in Fig. 6 for four different layer thicknesses. There is a steady rise in open circuit voltage with the increase in p-layer thickness and the maximum value (735.2 mV) is attained with 25nm layer thickness [Fig. 6(a)]. Completely reverse scenario is observed in case of short circuit current density characteristics, gradual decline of its value with increasing thickness [Fig. 6(b)]. Maximum power output from the cell and conversion efficiency curve show almost similar trend as the short circuit current and the maximum conversion efficiency is found with 10nm p-layer thickness [Fig. 6(c)-(d)]. Fill factor is also enhanced a great deal with increased p-layer thickness[Fig. 6(e)].

## *G. Effect of a:Si:H (n) layer doping concentration*

Fig. 7 lifts up the effect of varying n-doped amorphous Si layer doping concentration on solar cell performance . Open circuit voltage initially shows a positive slope with the increase of doping level, reaches maximum value (734.5mV) at $2x10^{19}$ $cm^{-3}$ and remains constant up to concentration level of $4x10^{19}$ $cm^{-3}$ and then there is a decline in open circuit voltage with increasing doping concentration [Fig. 7(a)]. Fig. 7(b) shows an initial rise of short circuit current density with increase in doping concentration up to $2x10^{19}$ $cm^{-3}$ ; then there is a less steep fall in current value up to $3x10^{19}$ $cm^{-3}$ and essentially remains constant with increasing doping concentration [Fig. 7(b)]. Maximum power output from the cell and conversion efficiency have almost similar characteristics as the short circuit current and the maximum conversion efficiency is attained with p-type doping concentration of $2x10^{19}$ $cm^{-3}$ [Fig. 7(c)-(d)]. Fill factor is initially dropped down a bit for doping level of $1x10^{19}$ $cm^{-3}$ to $2x10^{19}$ $cm^{-3}$, but it is enhanced for further increase of doping concentration [Fig. 7(e)].

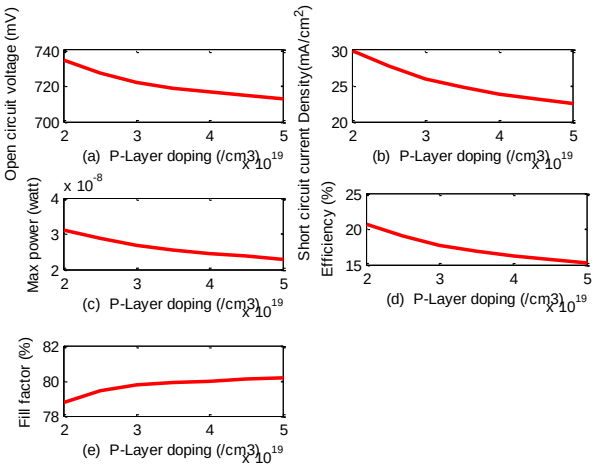


Fig. 5. Effect of a:Si:H (p) layer doping on device performance

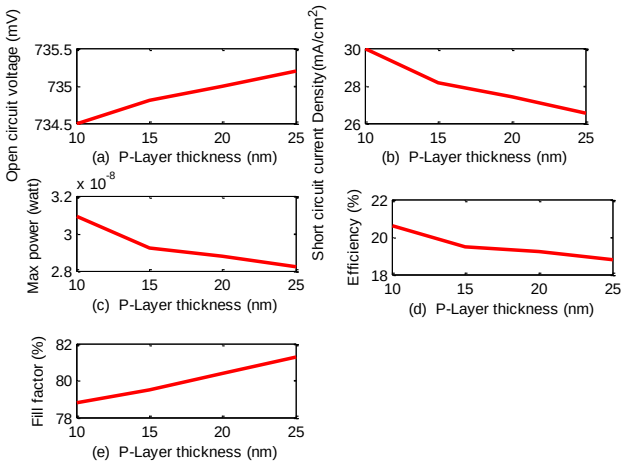


Fig. 6. Effect of a:Si:H (p) layer thickness on device performance

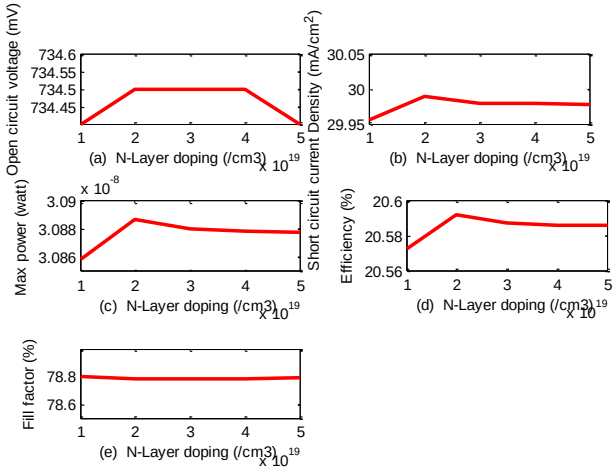


Fig. 7. Effect of a:Si:H (n) layer doping on device performance

## H. *Effect of a:Si:H (n) layer thickness*

Effect of n-doped amorphous Si layer thickness on HIT solar cell performance has been illustrated in Fig. 8 for five different n-layer thicknesses. It is obvious from Fig. 8(a) that open circuit voltage does not change a great deal with variation in the n-layer thickness, rather it moves up and down in the small voltage range of 734.5mV to 734.52mV. Short circuit current density remains constant up to 30nm layer thickness; then there is a rise in current density to the maximum value at layer thickness of 35nm [Fig. 8(b)]. From the maximum value, there is a sudden fall in short circuit current at 40nm, which remains constant for further increase in n-layer thickness. Maximum power output from the cell and conversion efficiency curve show almost identical trend as the short circuit current and maximum conversion efficiency is attained with 35nm n-layer thickness [Fig. 8(c)-(d)]. Fig. 8(e) illustrates that there is an initial fall in the value of Fill factor up to 30nm layer thickness; then there is a sudden rise in its value up to maxima of 78.78% at 35nm and again there is a decline in Fill factor thereafter [Fig. 8(e)].

## I. *Effect of TCO contact work function*

Impact of varying TCO contact work function on the device performance has been presented in Fig. 9 for four different contact workfunctions. Open circuit voltage and short circuit current density are significantly enhanced due to increase in contact work functions [Fig. 9(a)-(b)] . Maximum value of the open circuit voltage and short circuit current are found to be 734.5mV and 5.338x10$^{-8}$ A respectively in our simulation for contact work function of 5.5eV. Maximum power output from the cell and conversion efficiency are also improved with increasing contact workfunction [Fig. 9(c)-(d)]. Fill factor of the device is enhanced from around 60% to 78.78% for variation of contac work function in the range 5.2eV to 5.5eV [Fig. 9(e)].

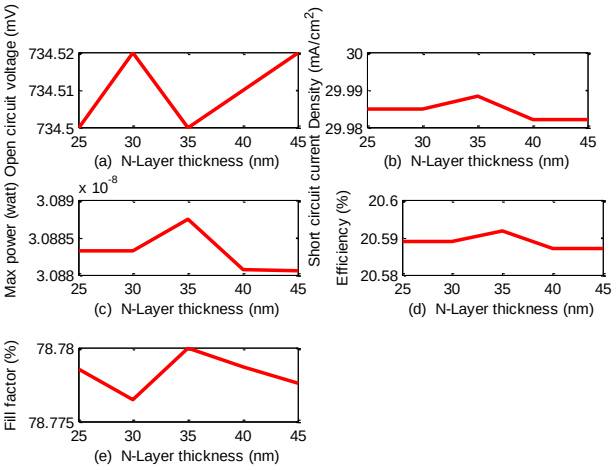


Fig. 8. Effect of a:Si:H (n) layer thickness on device performance

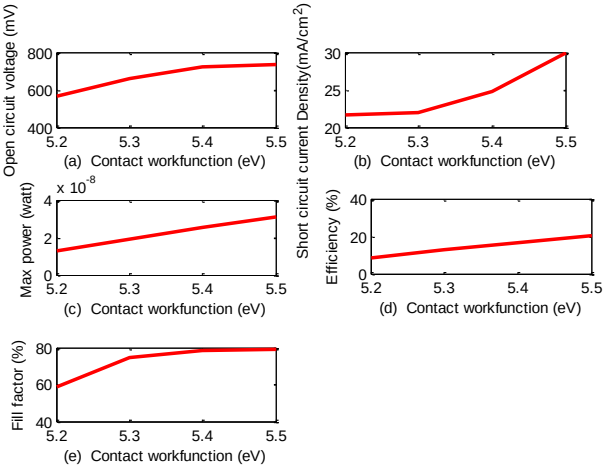


Fig. 9. Effect of TCO contact work function on device performance

## V. Conclusions

This work presents a simulation study of the device performance of a HIT solar cell due to varied device parameters like doping concentration, thickness, work function of different layers of the heterojunction device. Simulation results from 2D device simulator ATLAS were analyzed overall and optimized device parameters were traced out. Optimum conversion efficiency from the device was found to be 20.59% and the device structure bids fair to be a promising one in terms of conversion efficiency if textured surface is used which reduces reflection significantly from front and rear surface of the solar cell device.

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